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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,513	10/26/2001	Klaus-Peter Behrens	20 01 0631	6890

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EXAMINER
TORRES, JUAN A

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/032,513	Applicant(s) BEHRENS ET AL.	
	Examiner Juan A. Torres	Art Unit 2631	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 November 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attachment.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 11/07/2005 have been fully considered but they are not persuasive.

Regarding claim 1:

The Applicant contends, "In the Matsumoto patent, a timing signal generator TG provides all clocking throughout the system (FIG. 2, col. 5, lines 21 - 24; and FIG. 5, col. 7, lines 61 - 65). Whereas TG provides all clocking throughout the system, all of the clock signals are synchronous with one another.....Whereas in the Matsumoto patent all clocks are synchronous with one another, the system in the Matsumoto patent has no need for a synchronization circuit for transferring data between two asynchronous circuits. There is no reason, and therefore no motive, to modify the system of the Matsumoto patent to include the synchronizer of the Alston patent. That Accordingly, the cited combination of the Matsumoto and Alston patents is improper for purposes of a sectionlo3ta) rejection of claim 1. During the teleconference, the Examiner suggested that if the system of the Matsumoto patent was modified to provide clocks from more than a single generator, there would then be a motive for further modifying the system of the Matsumoto patent to include the synchronizer of the Alston patent. Applicants then explained that a modification of the Matsumoto patent to provide clocks from more than a single generator would be contrary to the Matsumoto patent's express teaching that TG provides all clocking throughout the system, thus changing the principle of operation of the system in the Matsumoto patent. Hence, the Matsumoto patent cannot

be modified to include the synchronizer of the Alston patent, for purpose of a section 103(a) rejection of claim 1.".

The Examiner disagrees and asserts, that, Matsumoto states (column 1 line e 33 to column 2 line 20): "The integration density in IC devices has been greatly increased in recent years. Accordingly, a large number of IC devices have been produced which have the following structure. That is, a memory circuit section and a multi-stage logic circuit section including a plurality of series-connected logic circuits cooperative with the memory circuit section are provided on a single chip to form an IC device. For example, an IC device includes a memory circuit section and such a multi-stage logic circuit section formed around the memory circuit section.

In such an IC device, plural logic stages in the multi-stage logic circuit section successively transmit a signal under control of a clock signal, and thus a time delay shift of the signal associated with the period of the clock signal is generated. Hence, the delay time of the output data signal from the to-be-measured IC device is different from the delay time of the expected signal from the IC tester, and moreover the difference in delay time between the output data signal and the expected signal varies. Thus, it is difficult to check the performance characteristics of the memory circuit section accurately.

In order to solve the above problem which arises in testing the memory circuit section of an IC device having a logic circuit section in addition to the memory circuit section, the following methods have hitherto been known.

For example, according to Japanese patent application JP-A-No. 59-119,595 (laid open on July 10, 1984), a circuit part operable in accordance with a predetermined clock signal in a test mode is formed in the IC device, **to synchronize the output data signal from the IC device with the expected signal, thereby eliminating the differences in delay time between the output data signal and the expected signal**. According to this method, the IC tester and the to-be-tested IC device are operated in synchronism with each other, and thus it can be prevented that the signal delay in the IC device is different from that in the IC tester. In this method, however, it is required to add a logic circuit section used only for testing the memory circuit section, to the IC device, and thus the whole of the IC device becomes large in scale and complicated in structure.

According to **another method, a circuit for putting a latch circuit**, which is included in the logic circuit section of a to-be-measured IC device to transfer an input signal under control of a clock signal, in a "through" state (that is, the state of the latch circuit capable of transferring the input signal thereto to the next stage without producing any delay time) is additionally provided, to prevent the signal delay in the IC device from being different from that in the IC tester. This method will be explained below in more detail, with reference to FIG. 1. "

And (column 3 lines 24-41):

"In an apparatus for testing an IC device in accordance with an embodiment of the present invention, the above-mentioned expected-signal transferring means **includes a plurality of transferring circuits, the number of which is equal to the**

number of clocked logic circuits on a test-signal transmission line in the IC device. Thus, the expected signal passes through transferring circuits, the number of which is equal to the number of clocked logic circuits included in the logic circuit section of the IC device for transferring the test signal (for example, the address and enable signals), to reach the comparing means. Accordingly, at the comparing means, the output signal of the IC device and the expected signal are synchronized with each other, that is, the output signal is equal in delay time to the expected signal. Thus, the performance characteristics of the IC device can be accurately checked without adding any special circuit to the IC device"

So Matsumoto synchronize the two signals using transferring means that includes a plurality of transferring circuits, the number of which is equal to the number of clocked logic circuits on a test-signal transmission line in the IC device, so he is using a latch circuit method.

Furthermore Matsumoto shows the use of two clocks in figures 5 and 6, an makes the synchronization in the same way, using latch circuits, because the two clock are out of phase: "FIG. 5 shows another embodiment of an apparatus for testing an IC device in accordance with an embodiment of the present invention. Referring to FIG. 5, the address signal A is transferred to the memory circuit section M of an IC device 51 through **latch circuits** 301, 302, 311 and 312 which are included in the logic circuit section L and are controlled by two clock signals ck_1 and ck_2 The clock signals ck_1 and ck_2 have the same repetition period but are different in phase from each other. Further, the enable signal EN is transferred to the memory circuit section M through latch circuits

321 and 322 which are controlled by the clock signals ck_1 and ck_2, and the output data signal from the memory circuit section M is transferred to the comparator circuit C through latch circuits 331 and 332 which are controlled by the clock signals ck_1 and ck_2". For these reasons and the reason stated en the previous Office action, the rejection of claim 1 is maintained.

Regarding claims 2-7:

The Applicant contends, ". Claims 2 - 7 depend from claim 1. By virtue of this dependence, claims 2 - 7 are also patentable over the cited combination of references.".

The Examiner disagrees and asserts, that, because the rejection of claim 1 is maintained, the rejection of claims 2-7 are also maintained. For these reasons and the reason stated en the previous Office action, the rejection of claims 2-7 are maintained.

Regarding claim 8:

The Applicant contends, "Claim 8 is an independent claim and includes recitals similar to those of claim 1, as described above. Thus, for reasoning similar to that provided in support for claim 1. Applicants submit that claim 8 is patentable over the cited combination of references.".

The Examiner disagrees and asserts, that, because the rejection of claim 1 is maintained, the rejection of claim 8 is also maintained. For these reasons and the reason stated en the previous Office action, the rejection of claim 8 is maintained.

Regarding claim 9:

The Applicant contends, "Claim 9 depends from claim 8. By virtue of this dependence, claim 9 is also patentable over the cited combination of references.".

The Examiner disagrees and asserts, that, because the rejection of claim 8 is maintained, the rejection of claim 8 is also maintained. For these reasons and the reason stated en the previous Office action, the rejection of claim 9 is maintained.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Matsumoto recognized the necessity of synchronization and provide different ways to do it (column 1 line e 33 to column 2 line 20), and he uses one of these ways using a latch circuit. Alston teaches another method of synchronization.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
11-14-2005

KEVIN BURD
PRIMARY EXAMINER